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International Office
INTERNATIONAL APPLICATION DISCLOSED BASED ON THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification[7]: H01L 29/78	A1	(11) International Publication No.: **WO 00/33385** (43) International Disclosure Date: June 8, 2000 (06/08/00)

(21) International Application No.: PCT/DE99/03542

(22) International Filing Date: Nov. 4, 1999 (11/04/99)

(30) Priority Data:
198 54 915.6, Nov. 27, 1998, (11/27/98) Germany

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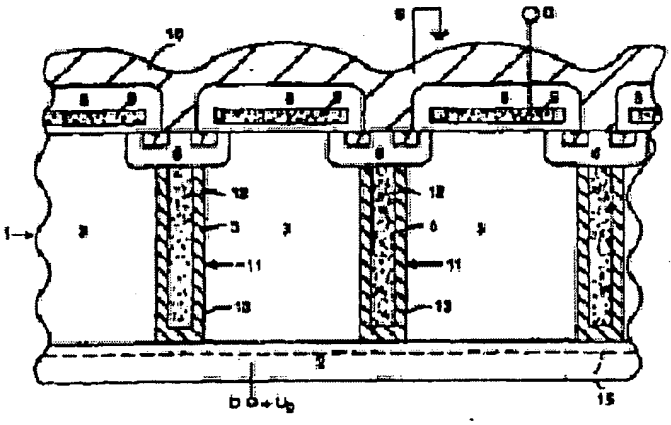
(81) Designated States: JP, KR, US, European Patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published:
With International Research Report.
Before expiration of the permissible deadline for amendments to the claims; to be published again if changes are submitted.

(54) Title: MOS FIELD EFFECT TRANSISTOR WITH AN AUXILIARY ELECTRODE



(57) Abstract [of the German original retranslated]

The invention concerns an MOS field effect transistor with a low on-state resistance R_{on} in which auxiliary electrodes (11) are provided in the drift path between the semiconductor zones (3) of the one conduction type, said auxiliary electrodes being composed of a polycrystalline silicon (12) that is coated with an insulating layer (5).

Description

MOS Field effect transistor with an auxiliary electrode

The current invention concerns a metal oxide semiconductor [MOS] field effect transistor with

-a semiconductor body of the one conduction type exhibiting a first and a second principal surface in which at least one first semiconductor zone of the other conduction type, or opposite of the one conduction type, is embedded,

-at least one second semiconductor zone of the one conduction type that is provided in the first semiconductor zone,

-a gate electrode at least in the region above the first semiconductor zone between the second semiconductor zone and the semiconductor body and

-a first electrode coming in contact with the semiconductor body on the second principal surface and with a second electrode at least coming in contact with the second semiconductor zone.

As is known, there has been an ongoing, long term search to find possible ways of reducing the on-state resistance R_{on} of MOS field effect power transistors (FETs) in particular. For example, in the US patent, US 5,216,275, a power semiconductor arrangement is described that is basically constructed in the manner initially described here: the drift path of this semiconductor device is provided with a so-called "voltage sustaining layer" that comprises vertical p- and n-conducting areas, in side by side alternation, and between which an insulating layer of silicon dioxide is provided. In Figure 4, a metal oxide semiconductor field effect transistor [MOSFET] is shown as an example of such a conventional semiconductor device.

This known MOSFET comprises a semiconductor body 1 with an n^+- conducting drain contact zone 2, with alternating n- conducting and p- conducting semiconductor zones 3 and/or 4 that are separated by an insulating layer 5 composed, for example, of silicon dioxide, with p- conducting semiconductor zones ("body" zones) 6 and with n- conducting semiconductor zones 7 which are embedded in zones 6.

For the semiconductor body 1, silicon is conventionally used although other materials can also possibly be applied. Also, it is possible to switch the arrangement of the types of conduction described here.

Gate electrodes 9 of doped polycrystalline silicon are embedded in an insulating layer 8, for example, of silicon dioxide or of silicon nitride and are provided with a terminal G. A metallic layer 10 of aluminum, for example, comes in contact with the n- conducting zones 7 and is provided with a source terminal S that can be grounded. On the n^+- conducting semiconductor layer 2, which is provided with a drain terminal D, is a drain voltage $+U_D$.

When the voltage is applied $+U_D$, the charge carriers in zones 3 and 4 are mutually depleted. If the total amount of n- type doping and p- type doping in these zones 3, 4, that run between the two principal surfaces of the semiconductor body 1 in the manner of columns, is about equal or low enough that these zones 3 and 4 are entirely depleted of charge carriers, before a breakdown sets in, then such a MOSFET can block high voltages and yet still continue to exhibit a low on-state resistance R_{on}. As a result of the insulating layer 5 between the n- conducting zones 3 and the p- conducting zones 4, the p- conducting zones 4 that are arranged beneath the zones 6 serve here as grounded magnetoresistive elements for the n- conducting zones 3, as long as the latter are not entirely depleted of charge carriers.

A MOSFET having the structure shown in Figure 4 is relatively elaborate to manufacture. This can be specifically attributed to the production of the insulating layers 5 and of the p- conducting zones 4 surrounded by said layers in an n- conducting semiconductor body 1.

It is therefore the objective of the current invention to create a MOSFET having a low on-state resistance such as that of the prior MOSFET, but which is substantially simpler to manufacture.

In accordance with the invention, this task is resolved for the initially described type of MOSFET in that at least one auxiliary electrode coated with an insulating layer is provided in the semiconductor body, said auxiliary electrode extending in the direction between the first and the second principal surface of the semiconductor body and being electrically connected with the first semiconductor zone. Preferably, the auxiliary electrode lies directly beneath the first semiconductor zone.

It is also possible to hereby provide several such auxiliary electrodes beneath each first semiconductor zone. These auxiliary electrodes can possibly be designed in the form of a "pencil". The auxiliary electrodes can extend as far as into one of the highly doped layers of a first type of conduction, that is into the proximity of a drain contact zone. But it is also possible that the auxiliary electrodes just reach only up to a weakly doped layer of one type of conduction, said layer being provided between the semiconductor body and a highly doped semiconductor layer, of one type of conduction, coming in contact with the first electrode.

The auxiliary electrode itself is composed of highly doped polycrystalline silicon while silicon dioxide is preferably used for the insulating layer.

The depth of the auxiliary electrodes can lie, for example, between 5 and 40 :m, while their width can range in the order of magnitude from 1 to 5 :m. The thickness of the insulating layer on top of the polycrystalline silicon of the auxiliary electrode can lie between 0.1 and 1 :m, whereby this thickness can increase in the direction of the second principal surface or toward the center of the auxiliary electrodes between the two principal surfaces.

The MOSFET, in accordance with the invention, can be manufactured in an especially simple manner; for example, in the n- conducting semiconductor bodies, trenches can be exemplarily incorporated by etching. The walls and the bases of these trenches are provided with an insulating layer that can be implemented by oxidation so that a silicon dioxide layer is formed as an insulating layer on the semiconductor body made of silicon. Thereafter, the trenches are filled with n^+- conducting or p^+- conducting polycrystalline silicon, which does not entail any problems.

For this, a p^+- type doping is preferred for the polycrystalline silicon of the auxiliary electrode; specifically, in the event that a hole might be present in the insulating layer, then a blocking pn-junction is effected through the hole in the n- conducting semiconductor body after a p-diffusion. In contrast, in the case of an n^+- type doping of the polycrystalline silicon of the auxiliary electrode, such a hole would create a short circuit for the n- conducting semiconductor body.

The auxiliary electrodes themselves can assume the shape of columns, grids or strips or even of other types of layout arrangements.

Also, the closer the auxiliary electrodes are arranged to one another, the higher the n- conducting semiconductors zones can be doped. However, one must take into consideration, in the case of auxiliary electrodes running mutually parallel, that the lateral surface charge of the n- conducting semiconductor zones is not to exceed a doping material quantity corresponding to more than double of the breakdown charge.

The n^+- type or p^+- type doping in the polycrystalline silicon of the auxiliary electrodes need not be homogeneous. Moreover, variations in the doping concentrations are permissible here without further ado. Nor is the depth of the auxiliary electrodes or of the trenches a critical factor: the latter may extend up to a highly doped drain contact zone, but are not required to do so.

In place of an exemplary n- conducting semiconductor body, layers with different degrees of doping can be provided for said semiconductor body.

In the following, the invention shall be described in detail by way of drawings. Shown in:

Figure 1 is a section through a MOSFET in accordance with a first exemplary embodiment of the invention,

Figure 2 is a section through a MOSFET in accordance with a second exemplary embodiment of the invention,

Figure 3 is a section through a MOSFET in accordance with a third exemplary embodiment of the invention,

Figure 4 is a section through a prior MOSFET.

Figure 4 has already been detailed in the introduction. In Figures 1 through 3, the same designations have been used to reference the various corresponding components as in Figure 4. The respectively provided types of conduction can be switched just as in Figure 4.

Figure 1 shows an exemplary embodiment of the MOSFET in accordance with the invention. In contrast to the conventional MOSFET in accordance with Figure 4, here there are no p-conducting zones 4 that are coated by an insulating layer 5. Moreover, in the MOSFET of the exemplary embodiment in figure 1, auxiliary electrodes 11 are provided that are respectively composed of n^+- type or p^+- type doped polycrystalline silicon 12 and that are coated with the insulating layer 5. In place of the polycrystalline silicon, another correspondingly conductive material can also possibly be used. The insulating layer 5 can also be composed of materials other than silicon dioxide such as for example silicon nitride, but also of various insulating films such as, for example, silicon dioxide or silicon nitride.

These auxiliary electrodes have an effect similar to the p- conducting zones 4 of the conventional MOSFET in Figure 4: when the drain voltage $+U_D$ is applied to the drain terminal D, the n-conducting zones 3 are depleted of their charge carriers. In this case, a greater field intensity in the electric field occurs on the insulating layer 5 than in the case of the MOSFET with the conventional structure in FIGURE 4. However, this has no effect on the targeted depletion of the charge carriers.

The fundamental advantage of the invention lies therein that the MOSFET in accordance with Figure 1 is substantially simpler to manufacture than the MOSFET in accordance with Figure 4: only trenches 13 need to be etched into the semiconductor body 1 approximately as deep as layer 2 and with a width of about 1 to 5 :m and a depth of about 5 to 40 :m, whose walls are then coated with the insulating layer 5 of silicon dioxide by oxidation, said layer thickness ranging from 0.1 to 1 :m. The thickness of the insulating layer 5 does not play any special role in this; said thickness can moreover gradually increase from the top in downward direction into the trenches 13 or also toward the trench center.

After this, the trenches are filled with the polycrystalline silicon 12 that can be doped for either the p^+- type or the n^+- type. However, a p^+- type doping of the auxiliary electrodes 11 is preferred in view of the fact that holes possibly present in the insulating layer 5 lead to greater efficiency, as has already been explained above.

The layout of the auxiliary electrodes 11 need not coincide with the arrangement of the individual semiconductor cells. Moreover, the auxiliary electrodes 11 can be provided in the shape of columns, grids or strips or can assume other types of layout arrangements.

In a preferred manner, the closer together the auxiliary electrodes 11 are to one another, the higher the n- conducting zones 3 will be doped. What remains essential in the case of auxiliary electrodes 11 running parallel to one another is just that the lateral surface charge of the n- conducting zones 3 does not exceed more than the double of the doping material quantity corresponding to the breakdown charge.

In place of the n- conducting zones 3 (or of the semiconductor body 1), several layers with varying doping concentrations can also be provided. Furthermore, the n^+- conducting zone 2 can also be replaced by an n-p^+- layer sequence or by an n^+-p^+- layer sequence, as this is suggested by the dashed line in Figure 1. In this case, we have an IGBT (IGBT = a bipolar transistor with an insulated gate).

Finally, the doping of the polycrystalline silicon 12 of the auxiliary electrodes 11 need not be homogeneous.

Figure 2 shows another exemplary embodiment of the invention in which, in contrast to the exemplary embodiment of Figure 1, two auxiliary electrodes 11 are arranged in each cell. Of course, it is also possible, given the case, to provide three or more auxiliary electrodes 11 for each cell.

Finally, it is also not requisite that the auxiliary electrodes 11 extend all the way to the highly doped n^+- conducting layer 2 on the side of the drain terminal D. Likewise, it is also possible that these auxiliary electrodes 11 already end at an n^+- conducting layer 14, which is provided between the n^+- conducting layer 2 and the n- conducting zones 3.

The invention makes it possible to create such an easily manufactured MOSFET with just the conventional steps required for trench production in semiconductor technology and still guarantees a low on-state resistance R_{on} in spite of the simplicity.

In the above exemplary embodiments, a vertical structure of the MOS field effect transistor in accordance with the invention is described. Of course, the invention can also be applied to a lateral structure as well in which the auxiliary electrodes 11 extend in a lateral direction in the semiconductor body.

Patent Claims

1. MOS Field effect transistor with

- a semiconductor body (1), being of one conduction type, exhibiting a first and a second principal surface, in which, on the face of the first principal surface, at least one first semiconductor zone (6) is embedded, said zone being of the conduction type opposite that of the first conduction type,

- a least a second semiconductor zone (7), being of one conduction type, that is provided in the first semiconductor zone (6),

- a gate electrode (9) at least in the region above the first semiconductor zone (6) between the second semiconductor zone (7) and the semiconductor body (1) and

- a first electrode (D) coming in contact with the semiconductor body (1) on the second principal surface and with a second electrode (10; S) coming at least in contact with the second semiconductor zone (7),

thus characterized in that

- in the semiconductor body (1) at least one auxiliary electrode (11) coated with an insulating layer (5) is provided that extends in the direction between the first and the second principal surface of the semiconductor body (1) and that is electrically connected with the first semiconductor zone (6).

2. MOS Field effect transistor in accordance with claim 1,

thus characterized,

that directly beneath each first semiconductor zone (6), one or several auxiliary electrodes (11) are provided.

3. MOS Field effect transistor in accordance with claim 1 or 2,

thus characterized,

that the auxiliary electrodes are fashioned in the form of a pencil.

4. MOS Field effect transistor in accordance with one of the claims 1 through 3,

thus characterized,

that the auxiliary electrodes (11) extend up to a strongly doped layer (2) of the one type of conduction in the region of the second principal surface.

5. MOS Field effect transistor in accordance with one of the claims 1 through 3,

thus characterized,

that the auxiliary electrodes (11) extend up to a weakly doped layer (14) of the one type of conduction, which is arranged between the semiconductor body (1) and a strongly doped semiconductor layer (2), of the one type of conduction, coming in contact with the first electrode (D).

6. MOS Field effect transistor in accordance with one of the claims 1 through 5,

thus characterized,

that the auxiliary electrode is composed of a highly doped polycrystalline silicon (12) that is coated with an insulating layer (5) of silicon dioxide.

7. MOS Field effect transistor in accordance with one of the claims 1 through 6,

thus characterized,

that the depth of the auxiliary electrodes (11) ranges from 5 to 40 :m.

8. MOS Field effect transistor in accordance with one of the claims 1 through 7,

thus characterized,

that the width of the auxiliary electrodes (11) ranges from about 1 to 5 :m.

9. MOS Field effect transistor in accordance with one of the claims 1 through 8,

thus characterized,

that the thickness of the insulating layer lies between 0.1 :m and 1 :m.

10. MOS Field effect transistor in accordance with one of the claims 1 through 9,

thus characterized,

that the thickness of the insulating layer (5) increases in the direction of the second principal surface.

11. MOS Field effect transistor in accordance with one of the claims 1 through 9, thus characterized, that the thickness of the insulating layer (5) increases progressively toward the middle of the auxiliary electrodes (11).

12. MOS Field effect transistor in accordance with one of the claims 1 through 11, thus characterized, that the auxiliary electrodes (11) are produced by etching in trenches (13) and filling said trenches with the insulating layer (5) and with polycrystalline silicon (12).

13. MOS Field effect transistor in accordance with claim 6, thus characterized, that the polycrystalline silicon (12) is not homogeneously doped.

14. MOS Field effect transistor in accordance with one of the claims 1 through 13, thus characterized, that on the semiconductor body (1), in the region of the second principal surface, a highly doped layer (2), being of the one type of conduction is provided, or a sequence of layers is provided comprising one layer, being of the one type of conduction, and of a highly doped layer, being of the other type of conduction, or a sequence of layers is provided comprising a highly doped layer of the one type of conduction and of a highly doped layer of the other type of conduction.